REMARKS

Reconsideration of the application is requested.

Claims 2-7, 23-34, and 37-38 are now in the application. Claims 37 and 38 have been amended. Claims 1, 8-22, and 35-36 had been canceled previously.

Claim Rejections – 35 U.S.C. § 101

The claims have once more been amended to assure that they satisfy the requirements of § 101. Instead of "using" the set of test patterns to test the IC, claims 37 and 38 now directly test the IC in the "testing" step. In addition, we have added an "outputting" step so as to ensure the understanding that the testing is not just done to manipulate numbers and other information, but to actually output a result of the testing step. This is, therefore, a tangible step and the testing sequence accomplishes a practical application. Support for the added terminology is found throughout the specification. Reference is had, for example, to the figures, where the results are output to a database (.vcm files) and/or the outputs are otherwise generated.

Reconsideration of the § 101 rejection is respectfully urged.

Claim Rejections – 35 U.S.C. §§ 102 and 103

We now turn to the art rejection, in which claims 2-7, 23-34, and 37-38 have been rejected as being anticipated by Yao's "Evolving Artificial Neural Networks" under 35 U.S.C. § 102. We respectfully traverse.

We submit that claims 37 and 38 are patentably distinguished over the teachings of Yao in that the set of selected test patterns is applied to the integrated circuit using an ATE as measurement system for semiconductors. Yao teaches how to use a GA (genetic algorithm) to improve the neural network learning phase.

The method of claims 37 and 38 on the other hand first adapts a neural network to approximate the behavior of an integrated circuit. Then we use a genetic algorithm on an ATE as measurement system for semiconductors, and not on the neural network itself. Yao does not teach anything about an ATE. In the Abstract on Page 1438, Section D, Yao does state that GAs can be used to tune circuit parameters. But he does not mention any use of an ATE. Yao does not disclose the use of any measurement system for semiconductors. He does not even disclose any other alternative testing system at all.

To briefly recap the applicable law: Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 221 USPQ 385 (Fed. Cir. 1984). W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303 (Fed. Cir. 1983).

Here, Yao fails to disclose, either expressly or under the principles of inherency, at least the required utilization of a genetic algorithm on an ATE as measurement system for semiconductors, in the context as claimed.

The methods of claim 37 and 38 require a genetic algorithm to be used on an ATE as measurement system, and not on the neural network itself. This is done by the steps (A) to (E). This applying of a genetic algorithm on an ATE is entirely novel.

The Examiner's careful listing of each of the claims and their juxtaposition against the teachings of Yao is appreciated. The main differences, however, appear to have been overlooked. To summarized the main difference once more: Yao teaches using a GA to improve a learning phase of the neural network. He does not disclose a measurement system, especially none for semiconductors. The methods defined in claims 37 and 38 first train a neural network, and then use data from the neural network and a GA on an ATE as measurement system for semiconductors. This is an entirely different way and concept of using both a neural network and a genetic algorithm.

The method of claim 37 and the computer-readable medium of claim 38 are not only novel but they are also non-obvious over Yao. Yao only mentions that neural networks can be fed with circuit parameters.

The methods of claim 37 and 38 now combine two different approaches to test integrated circuits: On the first hand a neural network, on the other hand a measurement system for semiconductors, an ATE. A central aspect of invention lies in combining these two different ways of testing integrated circuits. Additionally, a GA is used on the ATE. This renders the method so efficient and superior to all prior known testing methods (see, also, the description of Fig. 4, for further explanation).

There is no suggestion found in Yao that could lead one of ordinary skill in the art to the inventions defined in claims 37 and 38.

In summary, none of the references, whether taken alone or in any combination, either show or suggest the method features of claims 37 and 38. These claims are, therefore, patentable over the art. The remaining claims depend from the patentable claim 37 and they are, therefore, patentable as well.

In view of the foregoing, reconsideration and allowance of the claims are solicited.

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